CLAIMS

1. A decoder system, comprising:

an address input (42) for receiving an address signal representing any of a plurality of address values (D);

a plurality of intermediate nodes (44);

a decoder (40) responsive to the address signal and arranged to stimulate, for each address value, a respective combination of the intermediate nodes; and

a plurality of outputs (16, 18), each responsive to a respective group of the intermediate nodes such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group;

characterised in that:

the decoder is arranged to perform a plural-stage process in determining which of the intermediate nodes to stimulate in response to each address value, said plural-stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs.

2. A system as claimed in claim 1, wherein the decoder comprises a microprocessor (46) which is programmed to perform the plural-stage process.

3. A system as claimed in claim 1, wherein the decoder comprises hard-wired logic circuitry and/or arithmetic circuitry and/or look-up circuitry (54, 56) arranged to perform the plural-stage process.

4. A system as claimed in any preceding claim, wherein the plural-stage process comprises the determination of a word of a predetermined constant weight code.

5. A system as claimed in claim 4, wherein the plural-stage process comprises:

mapping or representing the address value in accordance with a mathematical structure;

performing one or more operations in the mathematical structure to provide results equivalent to generation of a word of a constant weight code; and

mapping or representing the results from the mathematical structure as a selection of intermediate nodes.

6. A system as claimed in claim 5, wherein the mathematical structure is a finite affine geometry.

7. A system as claimed in claim 5, wherein the mathematical structure is a finite projective geometry.

8. A system as claimed in claim 5, wherein the mathematical structure is a difference family and the one or more operations comprise arithmetic operations with sets of elements from a group.

9. A system as claimed in claim 5, wherein the mathematical structure is chosen such that that the one or more operations are in accordance with a concatenation scheme.

10. A system as claimed in any preceding claim, wherein, in response to each address value, a respective single one of the outputs is stimulated, or stimulated beyond a predetermined threshold.

11. A system as claimed in any of claims 1 to 9, including a resolution input for receiving a resolution signal representing any of a plurality of resolution values, and wherein the decoder is responsive to the resolution signal such that:-

when the resolution signal has a first value, the combination of intermediate nodes stimulated in response to each address value causes a first number of the outputs to be stimulated, or to be stimulated beyond a predetermined threshold; and

when the resolution signal has a second value, the combination of intermediate nodes stimulated in response to each address value causes a group of a second number of the outputs, greater than said first number, to be stimulated, or to be

stimulated beyond the threshold.

12. A system as claimed in claim 11, wherein the decoder is responsive to the resolution signal such that when the resolution signal has at least one further value, the combination of intermediate nodes stimulated in response to each address value causes a, or a respective, group of a further number of the outputs, greater than said first number or said second number, to be stimulated, or to be stimulated beyond the threshold.

13. A system as claimed in claim 12, wherein the or each further different number is an integer multiple of said second number.

14. A system as claimed in claim 13, wherein each group, when the resolution signal has said one further value, is a union of a predetermined number of the groups when the resolution signal has said second value.

15. A system as claimed in claim 12, wherein the or each further different number is an integer multiple of said first number.

16. A system as claimed in claim 15, wherein each group, when the resolution signal has said one further value, is a union of a predetermined number of the groups when the resolution signal has said first value.

17. A system as claimed in any of claims 11 to 16, wherein said first number is one.

18. A system as claimed in any of claims 11 to 17, wherein the arrangement is such that the outputs which are so stimulated in response to each address value when the resolution signal has said second value are physically grouped adjacent each other.

19. A system as claimed in any of claims 10 to 18 wherein, in response to each address value, all of the outputs not stimulated beyond the determined threshold are also

not stimulated beyond a second determined threshold, lower than the determined threshold.

20. A method of manufacturing a system as claimed in any preceding claim, comprising the steps of:-

providing such a decoder which is:-

responsive to an address signal representing any of a plurality of address values; and

arranged to stimulate, for each address value, a respective combination of intermediate nodes;

providing a plurality of outputs;

determining, for each output, a respective group of the intermediate nodes to which that output is to be responsive; and

rendering each output responsive to the intermediate nodes in the respective determined group such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group;

characterised by the steps of:-

determining a plural-stage process to be performed by a decoder, said plural-stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs;

arranging the decoder to perform the determined plural-stage process in determining which of the intermediate nodes to stimulate in response to each address value; and

using the determined plural-stage process in said step of determining the group of the intermediate nodes to which the outputs are to be responsive.

21. A method as claimed in claim 20, wherein the steps of providing such a decoder which is responsive to an address signal representing any of a plurality of address values and arranged to stimulate, for each address value, a respective combination of intermediate nodes, and of

determining, for each output, a respective group of the intermediate nodes to which that output is to be responsive are achieved by determination of a constant weight code,

wherein words of said constant weight code are used for determining respective combinations of intermediate nodes for each address value, wherein the plural-stage process performed by the decoder comprises the determination of a word of a predetermined constant weight code.

22. A method as claimed in claim 21, wherein the constant weight code is derived through mapping of address values into an affine geometry.

23. A method as claimed in claim 21, wherein the constant weight code is derived through mapping of address values into a projective geometery.

24. A method as claimed in claim 21, wherein the constant weight code is derived through representing the address values as the translates of the sets of a difference family.

25. A method as claimed in claim 21, wherein the constant weight code is derived through the method of concatenation of codes with the address values determining particular codewords used in the concatenation.